IN THE SPECIFICATION

Please amend the paragraph beginning on page 8, line 21 and ending on page 9, line 9 as follows:

(Presently Amended) In one embodiment, the present scheme involves simulating a photolithographic mask for fabrication of an integrated circuit, then simulating an image to be produced by that mask on a wafer. Afterwards, the mask may be corrected and/or optimized and/or the simulation or image thereof may be so corrected and/or optimized. ~~Such corrections/optimized.~~ Such correction/optimization may be accomplished by increasing or decreasing at least one magnitude or value of an optical proximity correction factor and/or a serif. The formats of the data input to or output ~~form~~from these simulation procedures are compatible with one another (e.g., bitmap format). Further, in other embodiments, corner rounding effects in an image produced by a mask may be corrected through simulation of optical proximity effects of the mask (e.g., effects of light having a wavelength approximately equal to four times a feature size-such as a line width or line spacing of the image). These corrections may be incorporated into the mask by adjusting an as-drawn layout of the mask as part of a CAD process.

Please amend the paragraph beginning on page 12, line 20 and ending on page 21, line 2 as follows:

(Presently Amended) Through examination of these overlays in accordance with the present methods, it has been observed that corner rounding of the reticle is on the order of 20 nm away from the drawn data (Figures 7A and 7C). This difference is reduced to below approximately 5 nm on the simulated contours (Figures 7B and 7D). Similar observations were made for both the SWL and DWL designs. The inside corners of the SWL design tended to simulate with slightly lower accuracy (approximately 10 nm from the actual drawn pattern), but still showing much improvement compared to the overlay of the SEM ~~reticel~~reticle to the drawn layout.